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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, LINH V	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 01/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/824,569	KAPLAN, TODD	
	Examiner	Art Unit	
	Linh V. Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-67 and 69* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4-17,20-33,48-67 and 69* is/are allowed.

6)☒ Claim(s) *2,3,18,19,34-36 and 41-47* is/are rejected.

7)☒ Claim(s) *37-40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to communication filed on 11/17/05. Claims 2 – 67 and 69 are pending on this application.

Response to Arguments

2. Applicant's arguments filed 11/17/05 regarding to claims 2, 34 and 41 have been fully considered but they are not persuasive.

Under remarks, with respect to claim 2, applicant argued that "analog element 131 in Fig. 14 is not part of the control arrangement", and further argued that "Examiner cannot backtrack the transformation occurring to signals INA and INB prior to entering the control arrangement in Robertson to conclude that the control arrangement comprises analog process elements". Examiner respectfully disagrees from the following:

The claimed invention is claiming for a control arrangement comprises analog process elements. The "comprises" wording in the claim is an opening language; therefore every element or electrical device, which coupling a system, is a part of that system. Per discussed, Fig. 7 of Robertson et al. teaches a system of control arrangement (X3, X1, X2) driving by signal IN B and IN A; wherein the signal IN A, IN B generated by analog process element 131 in Fig. 14. Therefore, clearly the analog process element 131 in Fig. 14 is part of control arrangement (X1, X2, X3) because the analog process element 131 is a driving source for control arrangement (X1, X2).

Under remarks, with respect to claim 34, applicant argued, "pipelining of signal involves delaying a signal (Website dictionary.com); and Roberson does not teaches pipelining or delay". Examiner respectfully disagrees from the following:

In Webster dictionary defined pipeline: *a processes through which supplies or as if from sources to user* and does not mention delaying a signal which indicated by applicant. Per explained, Fig. 7 and 6 of Roberson clearly teaches a pipeline (20): processes (through which supplier (INA, INB) or as if from sources (INA, INB) to user (OUTA, OUT B)).

Under remarks, with respect to claim 41, applicant argued, "Adams does not constitute a tuning arrangement to adjust a frequency spectrum of DAC errors". Examiner respectful disagrees from the following:

Fig. 13 of Adams clearly teaches a tuning arrangement [152] in conjunction with (150) to adjust a frequency spectrum of DAC (232) errors, thus shaping the DAC (132) errors away from a desired frequency band (Col. 3 lines 19 – 27 disclosing the rotating (152) in conjunction with scrambling (153) to allows one to manipulate the errors in power spectrum). Further more Fig. 4A – 4F teaches multiples adjustment for frequency spectrum can be made by the adjusting the steps per clock cycle of the rotating 152 (See Col. 5 lines 35 – 45).

Applicant's arguments, with respect to 69 have been fully considered and are persuasive. The rejection of claim 69 has been withdrawn.

Per discussed above, the references from previous office action are applying to this office action.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 2, 3, 18, 19, and 34 - 36, are rejected under 35 U.S.C. 102(b) as being anticipated by Robertson et al. U.S. Patent No. 6,124,813.

Regarding claim 2, Fig. 5 and 7 of Robertson et al. disclose a switching arrangement comprising: a digital input comprising a first digital input portion (In A) and a second digital input portion (In B); a digital output (output of 20) comprising a first digital output portion (Out A) and second digital output portion (Out B); a switching element (20) between the digital input (A, B) and the digital output (Out A, Out B), the switching element having a first condition (No Swap) allowing the first digital output portion (Out A) to correspond to the first digital input portion (A) and the second digital output portion (Out B) to correspond to the second digital input portion (B), and a second condition (Swap) allowing the first digital output portion (Out A) to correspond to the second digital input portion (B) and the second digital output portion (Out B) to

correspond to the first digital input portion (A) ; and a control arrangement (X1, X2, X3) to switch the switching element between the first condition and the second condition; a control arrangement (X1, X, X3) to switching (26) the switching element (20) between the first and second condition, wherein the control arrangement comprises analog processing elements (IN A, and IN B of the control arrangement X1, X2 are the output signals of analog processing elements of Flash Analog to Digital converter; See Fig. 14 [131]).

Regarding claim 3, wherein the control arrangement (X1 – X3) has a first control input (IN A) connected with the first digital input portion (A), a second control input (IN B) connected with the second digital input portion (B), and a control output (26), the control output (26) allowing the switching element to assume the second condition (Col. 5 lines 31 – 34) if the first digital input portion is different from the second digital input portion (Col. 4 lines 46 – 60).

Regarding claim 18, wherein the switching element is a multiplexer (Fig. 7[20] disclosing multiplexing system for transmitting multiple signals A and B; See Webster Dictionary for "multiplex").

Regarding claim 19, wherein the switching element is a latched multiplexer (Fig. 7[20] disclosing multiplexing system for transmitting multiple signals by using switches 24, 24 for engaging or latching the paths between input terminals [A, B] and output terminals [Out A, Out B]).

Regarding claim 34, Fig. 7 of Robertson et al. discloses a circuit comprising: a first input (A) and a second input (B); a control element (X1 – X3) connected with the

first input and second input; a switch (20) either switching or not switching (Col. 4 lines 46 – 60) the first input (A) and the second input (B) according to the control element (X1 – X3); and a clocking (CLK) arrangement to pipeline (See Fig. 6, and 7 for disclosing multiples "pipelines: *a processes through which supplies or as if from sources (IN) to user (OUT)*) the first and the second input switch (IN A, IN B).

Regarding claim 35, wherein the first input (A) and the second input (B) are digital inputs (Col. 8 lines 5 – 6).

Regarding claim 36, wherein the control element comprises a delta-sigma modulator (Fig. 1).

5. Claims 41 – 47 are rejected under 35 U.S.C. 102(e) as being anticipated by Adams et al. U.S. 6,614,377

Regarding claim 41, Fig. 13 of Adams et al. discloses a digital-to-analog converter (232) mismatch shaper (150) comprising: a first input (Fig. 4 disclose a detailed circuit of scrambler circuit 150 having first input [IN A]) and a second input (Fig. 4 [IN B]); a control element (Fig. 4 [X1 – X3) connected with the first input (IN A) and the second input (IN B); a switch (Fig. 4 [50]) either switching or not switching the first input and the second input according to the control element (Fig. 4[SELECT]); and a tuning arrangement (Fig. 13 [152]) to adjust a frequency spectrum of DAC errors, thus shaping the DAC errors away from a desired frequency band (See Fig. 14a – 14d).

Regarding claim 42, wherein the first input (Fig. 4 [IN A]) and the second input (Fig. 4 [IN B]) are digital inputs.

Regarding claim 43; wherein the control element comprises a delta-sigma modulator (Fig. 13).

Regarding claim 44, fig. 13 of Adams et al. further discloses wherein the delta-sigma modulator comprises a filtering element (212) and a quantizer (214).

Regarding claim 45, wherein the filtering element (212) comprises at leas one delay element (210) every electrical device using to transfer signal is a delay element to its input signal).

Regarding claim 45, wherein the filtering element (212) comprises at leas one delay element (every electrical device using to transfer signal is a delay element to its input signal).

Regarding claim 46, wherein the delay element comprises an adjustable gain circuit (the capacitor array is an adjustable gain circuit for the input signal. See Col. 1 lines 42 - 43).

Regarding claim 47, wherein the filter element (capacitor array) further comprises a plurality of transconductors (capacitor is a electrical conducting element use to transfer signal), and wherein the turning arrangement frequency (Fig. 13) adjusting at least one transcoductor of the plurality of transconductors (Col. 1 lines 42 – 43 disclosing multiple transconductors capacitors having adjusting switches).

With respect to claim 69, the prior art does not teach a first DAC having a first DAC input and a first DAC output; providing a second DAC having a second DAC input and a second DAC output; connecting the first circuit output with the first DAC input and the second circuit output with the second DAC input; subtracting the second DAC output

from the first DAC output to provide a difference output; and inputting the difference output to a spectrum analyzer.

Allowable Subject Matter

6. Claims 37 - 40, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. With respect to claim 37, in addition to other elements in the claim, the prior art does not teach wherein the clocking arrangement clocks the filter element and the quantizer.

7. Claims 4 – 17, 20 - 33, 48 – 52, and 53 – 67, and 69 are allowed.

The following is an examiner's statement of reasons for allowance:

With respect to claim 4, in addition to other elements in the claim, the prior art does not teach wherein the control arrangement comprises a subtractor, subtracting the first digital input portion from the second digital input portion, the subtractor having a subtractor output with a first subtractor output value if the first digital input portion is not in a predetermined relationship with the second digital input portion and a second subtractor output value if the first digital input portion is in a predetermined relationship with the second digital input portion.

With respect to claims 48 and 53, in addition to other elements in the respective claim, the prior art does not teach a control element to control switching of the switch, the control element connected with the evaluation element and the switching element, the control element comprising a quantizer having a quantizer output, wherein switching

between the first digital input and the second digital input depends on the quantizer output when the first digital input and the second digital input are in predetermined relationship therebetween and switching between the first digital input and the second digital input does not depend on the quantizer output when the first digital input and the second digital input are not in the predetermined relationship therebetween.

With respect to claim 69, the prior art does not teach a first DAC having a first DAC input and a first DAC output; providing a second DAC having a second DAC input and a second DAC output; connecting the first circuit output with the first DAC input and the second circuit output with the second DAC input; subtracting the second DAC output from the first DAC output to provide a difference output; and inputting the difference output to a spectrum analyzer.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

7. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Rexford Barnie can be reached at (571) 272-7492. The fax phone numbers for the organization where this application or proceeding is assigned are (571-273-8300) for regular communications and (571-273-8300) for After Final communications.

01/18/06

Linh Van Nguyen

Art Unit 2819